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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
ROBERTS, JESSICA M	

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2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,380	THANGARAJ ET AL.	
	Examiner	Art Unit	
	JESSICA ROBERTS	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/02/2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/02/10 has been entered.

Status of the Claims

Claims 1-15 are presently pending and claims 16-18 are cancelled.

Response to Arguments

As to Applicants argument regarding that since Figure 14 merely describes the stream, without any reference to how the stream is stored in memory, the foregoing does not teach "a start code starting at a byte in a middle portion of a data word in a memory".

The Examiner respectfully disagrees. As shown in Fig.13A, in each of higher layers from the sequence layer to the picture layer, each code boundary is byte assigned, [0119] and fig. 13A.

Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG

stream, [0277]. Since Sugiyama discloses the stream can be written in the memory and the VLC controls the address of the stream, it is clear to the examiner that Sugiyama discloses the stream is written to an address in memory. Therefore, since Sugiyama discloses the start codes are byte assigned and the streams can be written in the memory and VLC controls the address of the stream, it is clear to the examiner Sugiyama disclose the writing a start code in the middle portion of a data word in memory.

As to Applicants argument regarding that the combination would not be operable to for “fetching data from the memory starting from the byte in the middle portion of the data word”. Neither Sugiyama or Malladi show any way of "fetching data... *starting from the byte in the middle portion of the data word”*.

The Examiner respectfully disagrees. Malladi teaches writing a starting address associated with the byte in a table (writing to a start code table, column 4 line 25-30) and fetching data from the memory starting from the bye (One the start code table has the identifying time stamp information, a CPU will periodically poll the start code table by communicating through a BIU that is connected to CPU BUS, and is connected to a BIU associated with the stream interface, column 15 line 39-41). Sugiyama teaches writing the start code to a middle of a data word (As shown in Fig.13A, in each of higher layers from the sequence layer to the picture layer, each code boundary is byte assigned, [0119] and fig. 13A. Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052].

Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]. Since Sugiyama discloses the stream can be written in the memory and the VLC controls the address of the stream, it is clear to the examiner that Sugiyama discloses the stream is written to an address in memory).

Therefore, since Sugiyama discloses the start codes are byte assigned and the streams can be written in the memory and VLC controls the address of the stream, it is clear to the examiner Sugiyama disclose the writing a start code in the middle portion of a data word in memory.

Since Malladi writes and fetches (polls) to the start code table, which would include the address (or location) of the start code and Sugiyama writes the start code to a middle portion of the data word, it is clear to the examiner, that Malladi (modified by Sugiyama) fully capable of fetching the start code from the byte in the middle of the data word, which reads upon the claimed limitation.

As to Applicants argument that that Son, column 8 line 53-56 merely states that "upon beginning a next start code 405 detection operation to detect next start code 405, multi-standard start code detector system 300 rapidly discards entire bit groups until detection of at least a portion of next start code 405". Assignee traverses because the foregoing does not teach the claimed “masking register”.

The Examiner respectfully disagrees. The Examiner respectfully disagrees. In addition Malladi teaches an arithmetic logic unit for performing a logical AND operation between a first one of the plurality of data words in the buffer and the first masking register (Malladi, column 9 line 48-51. The examiner notes that an ALU has been able to perform both the logical operation of AND/OR on the chip level).

Claim Objections

2. Claim 1 is objected to because of the following informalities:

3. Re claim 1, line 14 "decompressin" should be changed to "decompressing". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., US-5, 815,206 in view of Hrusecky et al., US-5,973,740 in view of Sugiyama et al., US- US-2003/00009722 and in further view of AAPA (herein referenced as Applicants Admitted Prior Art).

Regarding claim 1, Malladi teaches A method for decoding video data, said method comprising: writing a starting address associated with the byte in a table <u>by said transport processor</u> (column 4 line 25-29 and fig. 4); fetching data from the memory starting from the byte (column 15 line 39-41 and fig. 4<u>) by a video decompression engine, said video decompression engine decompressin the data from the memory starting from the byte in the middle portion of the data word, thereby resulting in decompressed video data; and writing the decompressed video data to a frame buffer</u> (Fig. 4 is a schematic diagram illustrating the hardware layout and signal interfaces of an audio and video decoder designed in accordance with one embodiment, col. 14 line 56-59 and fig. 4). Malladi is silent in regard to writing a start code starting at a byte in a middle portion of a data word in a <u>compressed data buffer</u> memory; and fetching data from the memory starting from the byte in the middle portion of the data word <u>by a video decompression engine, said video decompression engine decompressin the data from the memory starting from the bye in the middle portion of the data word, thereby resulting in decompressed video data.</u>

However, Hrusecky teaches fetching data from memory by a video <u>decompression engine</u> (Fig. 4 clearly discloses where the video decoder (54) fetches data from the DRAM (53) using the memory controller (52), fig. 4 elements 52, 53, 54),

said video decompression engine (fig. 4 element 54) decompressin the data from the memory (MPEG compressed video data is then retrieved by the video decoder 54 from the DRAM 53 and decoded, col.8 line 42-45) thereby resulting in decompressed video data (fig. 4) and writing the decompressed video data to a frame buffer (col. 8 line 45-49).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hrusecky with Malladi for providing improved memory management.

Malladi (modified by Hrusecky) as a whole is silent in regards to writing a start code starting at a byte in a middle portion of a data word.

However, Sugiyama teaches to writing a start code starting at a byte in a middle portion of a data word in a memory (Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]. Since Sugiyama discloses the stream can be written in the memory and the VLC controls the address of the stream, it is clear to the examiner that Sugiyama discloses the stream is written to an address in memory. Therefore, since Sugiyama discloses the start codes are byte assigned and the streams can be written in the memory and VLC controls the address of the stream, it is clear to the examiner Sugiyama disclose the writing a start code in the middle portion

of a data word in memory, reading upon the claimed limitation); and fetching data from the memory starting from the byte in the middle portion of the data word (Sugiyama teaches writing the start code to a middle portion of a data word, (Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]). Malladi teaches writing a starting address associated with the byte in the table (writing to a start code table, column 4 line 25-30) and fetching data from the memory starting from the byte (once the start code table has the identifying stamp information, a CPU will periodically poll the start code table by communicating through a BIU that is connected with stream interface, column 15 line 39-41)).

Since Malladi writes and fetches (polls) to the start code table, which would include the address (or location) of the start code and Sugiyama writes to the start code to a middle portion of the data word, it is clear to the examiner that Malladi (modified by Sugiyama) is fully capable of fetching the start code from the byte in the middle of the data word, which reads upon the claimed limitation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyama to provide a stream processing apparatus that stably operates even if an invalid VLC that is not

contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Malladi (modified by Hrusecky and Sugiyama) is silent in regards to a compressed data buffer, a transport processor.

However, AAPA teaches a compressed data buffer (AAPA discloses that when a decoding system received video data for decoding, the decoding system places the video data in to a decompressed data buffer, [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of AAPA with Malladi (modified by Hrusecky and Sugiyama) for providing improved image processing.

Regarding claim 2, Malladi (modified by Hrusecky, Sugiyama, AAPA) as a whole teaches everything claimed as applied above (see claim 1). In addition, Malladi teaches wherein the start code is associated with a slice (Malladi, column 8 line 32-34).

Regarding claim 3, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 1). Sugiyama further teaches wherein the data word comprises at least 16 bytes (Sugiyama, fig. 14). Therefore, it would have been obvious for one of ordinary skill I the art at the time of the invention to combine the teaching of Malladi (modified by Hrusecky and AAPA) with Sugiyamas' teaching of a data word of at 16 bytes to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 4, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole further teach writing another start code to another byte (Malladi teaches more than one start code, column 10 line 63-65) in a middle portion of another data word in the memory (Sugiyama, fig. 14); writing another address associated with the another byte in the table (Malladi, column 10 line 60-67); and wherein fetching data from the memory starting from the byte further comprises: fetching data from the memory starting from the byte and ending with a byte preceding the another byte (Malladi, column 15 line 39-41. It would be obvious that the system as disclosed by Malladi would be fully capable of fetching data from the memory starting from the byte and ending with a byte preceding the another byte, as the system checks for another start code (column 10 line 66-67), and if there is no start code, the process simply returns to decoding macroblocks as indicated (column 11 line 1-2). Further, the examiner notes that the byte at the end of the start code would be the byte preceding another start code.

Regarding claim 5, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole further teaches looking up the address in the table (Malladi teaches writing to the start code table, column 4 line 25-29. The examiner notes that since Malladi teaches writing to the start code table, it is clear that in order for Malladi to use the start codes, it would necessitate looking up the address from the start code table).

Regarding claim 6, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole further teaches where looking up the another address in the table (Malladi teaches writing to the start code table, column 4 line 25-29 The examiner notes that since Malladi teaches writing to the start code table, it is clear that in order for Malladi to

use the start codes, it would necessitate looking up the address from the start code table).

Regarding claim 7, Malladi teaches system for decoding video data (abstract and column 1 line 24-26), said system comprising: a memory comprising a plurality of data words (Malladi, start code table, fig. 4), for storing a start code (fig. 4); a table for storing a starting address associated with the byte (Malladi, fig. 4); and a direct memory access module for providing data from the memory starting from the starting address (Malladi, column 21-24). Malladi is silent in regards to a compressed data buffer the start code starting at a byte in a middle portion of a particular one of the data words; the starting address in the middle portion of the data word; a video decompression engine for decompressing the data from the memory starting from the starting address in the middle portion of the data word, thereby resulting in decompressed video data; and a frame buffer for storing the decompressed video data.

However, Hrusecky teaches a memory access module for providing data from a memory by a video decompression engine (Fig. 4 clearly discloses where the video decoder (54) has access to the DRAM by the memory controller (52) , fig. 4 elements 52, 53, 54) for decompressing the data from the memory (MPEG compressed video data is then retrieved by the video decoder 54 from the DRAM 53 and decoded, col.) thereby resulting in decompressed video data (fig. 4); and a frame buffer for storing the decompressed video data (fig. 5 element 107).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hrusecky with Malladi for providing improved memory management.

Malladi (modified by Hrusecky) is silent in regards the start code starting at a byte in a middle portion of a particular one of the data words; the starting address in the middle portion of the data word.

However, Sugiyama teaches the start code starting at a byte in a middle portion of a particular one of the data words (fig. 14); the starting address in the middle portion of the data word (Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]). Malladi teaches writing a starting address associated with the byte in the table (writing to a start code table, column 4 line 25-30) and fetching data from the memory starting from the byte (once the start code table has the identifying stamp information, a CPU will periodically poll the start code table by communicating through a BIU that is connected with stream interface, column 15 line 39-41)).

Since Malladi writes and fetches (polls) to the start code table, which would include the address (or location) of the start code and Sugiyama writes to the start code to a middle portion of the data word, it is clear to the examiner that Malladi (modified by

Sugiyama) is fully capable of the starting the address in the middle portion of the data word.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyama to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Malladi (modified by Hrusecky and Sugiyama is silent in regards to compressed data buffer, a transport processor.

However, AAPA teaches a compressed data buffer (AAPA discloses that when a decoding system received video data for decoding, the decoding system places the video data in to a decompressed data buffer, [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of AAPA with Malladi (modified by Hrusecky and Sugiymama) for providing improved image processing.

Regarding claim 8, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition, Malladi teaches a video transport processor (Malladi, fig. 4:417) for writing the start code starting at a byte in a middle portion of the particular data word in the memory (Sugiyama, fig. 14).

Regarding claim 9, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition, Malladi

wherein the start code is associated with a slice (Malladi, start code, column 8 line 32-34 and fig. 1A).

Regarding claim 10, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole teaches everything claimed above (see claim 7). Malladi is silent in regards to the data word comprises at least 16 bytes.

However, Sugiyama teaches the data word comprises at least 16 bytes (Sugiyama, fig. 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Malladi (modified by Hrusecky and AAPA) with Sugiyamas' teaching of the data word comprising at least of 16 bytes to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 11, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole further teaches wherein the video transport processor (Malladi, fig. 4:417) writes another start code (Malladi, teaches more than one start code, column 10 line 63-65) in the memory and wherein the table stores another address associated with the another byte in the table (Malladi, start code table, fig. 4) and wherein the direct memory access module fetches data from the memory starting from the byte and ending with a byte preceding the another byte (Malladi, column 15 line 39-41. It would be clear that the system as disclosed by Malladi would be fully capable of fetching data from the memory starting from the byte and ending with a byte preceding the another byte, as the system

checks for another start code (column 10 line 66-67), and if there is no start code, the process simply returns to decoding macroblocks as indicated (column 11 line 1-2). Further, it is clear that the byte at the end of the start code would be the byte preceding another start code). Malladi is silent in regards to another byte in a middle portion of another data word.

However, Sugiyama teaches another byte in a middle portion of another data word (Sugiyama, fig. 14)

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi (modified by Hrusecky and AAPA) with Sugiyamas' teaching of a start code in the middle of a data word to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 12, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition Malladi teaches a master processor for looking up the address in the table (Malladi, column 15 line 38-42).

Regarding claim 13, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition Malladi wherein the master processor looks up the another address in the table (Malladi, teaches writing more than one start code, column 10 line 60-67. The examiner notes,

since Malladi writes more than one start code, and it polls the entire start code table, it is clear that more than one address is looked up, Malladi, column 15 lines 38-42).

Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., US-5, 815,206 in view of Hrusecky et al., US-5,973,740 in view of Sugiyama et al., US- US-2003/00009722 and in further view of AAPA and further view of Son et al., US-5, 898,897.

Regarding claim 14, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything as claimed above, see claim 7. In addition, Malladi teaches wherein the direct memory access module (Malladi, column 21-24) further comprises: a buffer comprising a plurality of data words for storing the video data from the starting address (Malladi, Malladi discloses where the parameters are loaded into a predefined memory location, column 7 line 63 to column 8 line 1-8. Further, Malladi discloses this process is done for multiple start codes, column 8 line 15-42); the first masking register (Malladi, column 3 line 65 to column 4 line 1-5); a first masking register (Malladi, column 3 line 65 to column 4 line 1-5). Malladi is silent in regards to a plurality of bytes corresponding to byte positions of the data words (Sugiyama, the slice start code contains the vertical position, [¶0110]. Further, Sugiyama discloses that each code boundary is byte assigned, and in the slice layer only the slice start code is byte assigned [¶0019]. The examiner notes that since each code word code is byte assigned, it would be obvious that the code words would include the byte positions); a byte position that is less than the four least significant bits of the starting address are

loaded with a first value and wherein each byte of the plurality of bytes in the first mask register that corresponds to a byte position that is equal or greater than the four least significant bits of the starting address are load with a second value (Sugiyama, [¶0359]. Since Malladi discloses loading of parameters column 7 line 63 to column 8 line 1-8, and Sugiyama discloses the vertical position information ranges from [00 00 01 01] to [00 00 01 AF], the combination of Malladi and Sugiyama as a whole would be fully capable of loading a first and second address to a register or memory dependent upon the least significant bits). The combination of Malladi and Sugiyama as a whole are silent in regards to a first masking register for discarding a portion of a first data structure that precedes the starting address; a state machine for loading the first masking register. However, Son discloses a first masking register for discarding a portion of a first data structure that precedes the starting address (Son, column 8 line 53-56); a state machine (Son, fig. 3:307) for loading the first masking register with a pattern wherein each byte of the plurality of bytes in the first mask register (Son, column 10 line 30-40). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi and Sugiyama with the teachings of Son for providing detection of signal features such as a start code in a bit stream that may be formatted in accordance with any of a plurality of formatting standards.

Regarding claim 15, Malladi (modified by Hrusecky, Sugiyama, AAPA and Son) as a whole teaches everything as claimed above (see claim 7). In addition Malladi teaches an arithmetic logic unit for performing a logical AND operation between a first

one of the plurality of data words in the buffer and the first masking register (Malladi, column 9 line 48-51. The examiner notes that an ALU has been able to perform both the logical operation of AND/OR on the chip level).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSICA ROBERTS whose telephone number is (571)270-1821. The examiner can normally be reached on 7:30-5:00 EST Monday-Friday, Alt Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marsha D. Banks-Harold/
Supervisory Patent Examiner, Art Unit 2621

/Jessica Roberts/
Examiner, Art Unit 2621